CLAIMS

1. A Schottky diode, comprising:

a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of a same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer, said semiconductor body defining a lower contact surface and a plurality of mesas projecting upwardly from said lower contact surface, said lower contact surface including at least a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and defining an upper contact surface, each of said plurality of mesas being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface;

a plurality of upper metallic contacts each disposed atop a respective one of said plurality of mesas and forming a respective Schottky contact with the upper contact surface of that mesa; and

one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact therewith, at least part of said one or more lower metallic contacts extending between at least some of said plurality of mesas.

2. A Schottky diode as claimed in claim 1 wherein a size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized.

3. A Schottky diode as claimed in claim 1 wherein each of said plurality of mesas includes a portion of said lower layer.

4. A Schottky diode as claimed in claim 1 wherein each of said plurality of upper metallic contacts includes a contact metal layer that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

5. A Schottky diode as claimed in claim 1 wherein each of said one or more lower metallic contacts includes a

contact metal layer that forms the ohmic contact with said lower contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

6. A Schottky diode as claimed in claim 1 wherein said one or more lower metallic contact regions includes one or more continuous regions, each such continuous region extending between two or more of said mesas.

7. A Schottky diode as claimed in claim 1 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

8. A Schottky diode as claimed in claim 1 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

9. A Schottky diode as claimed in claim 1 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.

10. A Schottky diode as claimed in claim 1 wherein said lower semiconductor layer and said upper semiconductor layer are n-type.

11. A Schottky diode as claimed in claim 1 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a convoluted perimeter.

12. A Schottky diode as claimed in claim 11 wherein said perimeter of said shape is at least two times a perimeter of a smallest theoretical rectangle enclosing said shape.

13. A Schottky diode as claimed in claim 1 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion and a plurality of extensions extending from said main portion, said plurality of extensions being interdigitated with regions of said lower contact surface.

14. A Schottky diode as claimed in claim 13 wherein said main portion is elongated at least in a first direction and at least some of said plurality of extensions are elongated in a second direction transverse to said first direction.

15. A Schottky diode as claimed in claim 13 wherein at least some of said plurality of extensions have length-to-width ratios of at least about 2:1.

16. A Schottky diode as claimed in claim 13 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

17. A Schottky diode as claimed in claim 13 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

18. A Schottky diode as claimed in claim 1 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion, at least one bridge extending from said main portion and a plurality of extensions extending from said bridge; said plurality of extensions being interdigitated with regions of said lower contact surface.

19. A Schottky diode as claimed in claim 18 wherein said main portion and said bridge are elongated at least in a first direction and at least some of said extensions are elongated in a second direction transverse to said first direction.

20. A Schottky diode as claimed in claim 18 wherein at least some of said extensions have length-to-width ratios of at least about 2:1.

21. A Schottky diode as claimed in claim 18 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

22. A Schottky diode as claimed in claim 18 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

23. A diode assembly including: a Schottky diode as claimed in claim 1, one or more first conductors electrically connected to at least some of said plurality of upper metallic

contacts and one or more second conductors electrically connected to one or more of said one or more lower metallic contacts.

24. A diode assembly as claimed in claim 23 wherein said one or more first conductors are electrically connected to all of said upper metallic contacts, and said one or more second conductors are electrically connected to all of said one or more lower metallic contacts.

25. A diode assembly as claimed in claim 24 wherein one or more second conductors are electrically connected to each said one or more continuous regions at a plurality of spaced-apart connection points.

26. A diode assembly as claimed in claim 25 wherein at least some of said connection points are disposed away from said mesas.

27. A diode assembly as claimed in claim 26 wherein at least some of said connection points are disposed between at least some of said mesas.

28. A diode assembly as claimed in claim 23 wherein said one or more first conductors and said one or more second conductors include interconnect bumps.

29. A diode assembly as claimed in claim 23 further comprising a submount structure including:

a submount substrate,

one or more first submount contacts, each such one or more first submount contacts being electrically connected to one or more of said one or more said first conductors and exposed at a front surface of said submount substrate, and

one or more second submount contact pads, each such one or more second submount contact pads being electrically connected to one or more of said one or more second conductors and exposed at said front surface of said submount substrate;

said semiconductor body being mounted on said front surface of said submount substrate in a flip-chip arrangement such that said first submount contacts are connected to said upper contacts and said second submount contacts are connected to said one or more lower contacts.

30. A diode assembly as claimed in claim 29 wherein said submount structure includes a first terminal and a second

terminal each disposed on said front surface of said submount substrate and configured to provide connections external to said assembly, each said one or more first submount contacts being electrically connected to said first terminal, and each said one or more second submount contacts being electrically connected to said second terminal.

31. A diode assembly as claimed in claim 29 wherein said submount structure includes a first terminal and a second terminal each disposed on a back surface of said submount substrate and configured to provide connections external to said assembly, each said one or more first submount contacts being electrically connected to said first terminal, and each said one or more second submount contacts being electrically connected to said second terminal.

32. A diode assembly as claimed in claim 31 wherein said submount structure includes at least a first conducting via that extends through said submount substrate and electrically connects each said one or more first submount contacts with said first terminal, and at least a second conducting via that extends through said submount substrate and electrically connects each said one or more second submount contacts with said second terminal.

33. A diode assembly as claimed in claim 32 wherein said submount structure includes a first common terminal and a second common terminal each disposed on said front surface of said submount substrate, said first common terminal electrically connecting each said one or more first submount contacts to said first conducting via, said second common terminal electrically connecting each said one or more second submount contacts to said second conducting via.

34. A Schottky diode, comprising:

a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of the same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer, said semiconductor body defining a lower contact surface and a plurality of mesas projecting upwardly from said lower contact

surface, said lower contact surface including a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and a further portion of said lower layer, each of said plurality of mesas defining an upper contact surface and being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface;

a plurality of upper metallic contacts each disposed atop a respective one of said plurality of mesas and forming a respective Schottky contact with the upper contact surface of that mesa; and

one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact therewith.

35. A Schottky diode as claimed in claim 34 wherein a size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized.

36. A Schottky diode as claimed in claim 34 wherein the distance between a top surface of said one or more lower metallic contacts and said lower contact surface is less than the distance between a bottom surface of said upper layer and said lower contact surface.

37. A Schottky diode as claimed in claim 34 wherein each of said plurality of upper metallic contacts includes a contact metal layer that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

38. A Schottky diode as claimed in claim 34 wherein each of said one or more lower metallic contacts includes a contact metal layer that forms the ohmic contact with said lower contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

39. A Schottky diode as claimed in claim 34 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

40. A Schottky diode as claimed in claim 34 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

41. A Schottky diode as claimed in claim 34 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.

42. A Schottky diode as claimed in claim 34 wherein said lower semiconductor layer and said upper semiconductor layer are n-type.

43. A Schottky diode as claimed in claim 34 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a convoluted perimeter.

44. A Schottky diode as claimed in claim 43 wherein said perimeter of said shape is at least two times a perimeter of a smallest theoretical rectangle enclosing said shape.

45. A Schottky diode as claimed in claim 34 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion and a plurality of extensions extending from said main portion, said plurality of extensions being interdigitated with regions of said lower contact surface.

46. A Schottky diode as claimed in claim 45 wherein said main portion is elongated at least in a first direction and at least some of said plurality of extensions are elongated in a second direction transverse to said first direction.

47. A Schottky diode as claimed in claim 45 wherein at least some of said plurality of extensions have length-to-width ratios of at least about 2:1.

48. A Schottky diode as claimed in claim 45 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

49. A Schottky diode as claimed in claim 45 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

50. A Schottky diode as claimed in claim 34 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape

having a main portion, at least one bridge extending from said main portion and a plurality of extensions extending from said bridge; said plurality of extensions being interdigitated with regions of said lower contact surface.

51. A Schottky diode as claimed in claim 50 wherein said main portion and said bridge are elongated at least in a first direction and at least some of said extensions are elongated in a second direction transverse to said first direction.

52. A Schottky diode as claimed in claim 50 wherein at least some of said extensions have length-to-width ratios of at least about 2:1.

53. A Schottky diode as claimed in claim 50 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

54. A Schottky diode as claimed in claim 50 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

55. A diode assembly including: a Schottky diode as claimed in claim 34, one or more first conductors electrically connected to at least some of said plurality of upper metallic contacts and one or more second conductors electrically connected to one or more of said one or more lower metallic contacts.

56. A diode assembly as claimed in claim 55 wherein said one or more first conductors are electrically connected to all of said upper metallic contacts, and said one or more second conductors are electrically connected to all of said one or more lower metallic contacts.

57. A diode assembly as claimed in claim 56 wherein one or more second conductors are electrically connected to each said one or more continuous regions at a plurality of spaced-apart connection points.

58. A diode assembly as claimed in claim 57 wherein at least some of said connection points are disposed away from said mesas.

59. A diode assembly as claimed in claim 58 wherein at least some of said connection points are disposed between at least some of said mesas.

60. A diode assembly as claimed in claim 55 wherein said one or more first conductors and said one or more second conductors are interconnect bumps.

61. A diode assembly as claimed in claim 55 further comprising a submount structure including:

a submount substrate,

one or more first submount contacts, each such one or more first submount contacts being electrically connected to one or more of said one or more said first conductors and exposed at a front surface of said submount substrate, and

one or more second submount contact pads, each such one or more second submount contact pads being electrically connected to one or more of said one or more second conductors and exposed at said front surface of said submount substrate;

said semiconductor body being mounted on said front surface of said submount substrate in a flip-chip arrangement such that said first submount contacts are connected to said upper contacts and said second submount contacts are connected to said one or more lower contacts.

62. A diode assembly as claimed in claim 61 wherein said submount structure includes a first terminal and a second terminal each disposed on said front surface of said submount substrate and configured to provide connections external to said assembly, each said one or more first submount contacts being electrically connected to said first terminal, and each said one or more second submount contacts being electrically connected to said second terminal.

63. A diode assembly as claimed in claim 61 wherein said submount structure includes a first terminal and a second terminal each disposed on a back surface of said submount substrate and configured to provide connections external to said assembly, each said one or more first submount contacts being electrically connected to said first terminal, and each said one or more second submount contacts being electrically connected to said second terminal.

64. A diode assembly as claimed in claim 63 wherein said submount structure includes at least a first conducting via that extends through said submount substrate and electrically connects each said one or more first submount contacts with said first terminal, and at least a second conducting via that extends through said submount substrate and electrically connects each said one or more second submount contacts with said second terminal.

65. A diode assembly as claimed in claim 64 wherein said submount structure includes a first common terminal and a second common terminal each disposed on said front surface of said submount substrate, said first common terminal electrically connecting each said one or more first submount contacts to said first conducting via, said second common terminal electrically connecting each said one or more second submount contacts to said second conducting via.

66. A submount structure, comprising:

a submount substrate;

one or more first submount contacts, each such one or more first submount contacts being exposed at a front surface of said submount substrate;

a first common terminal disposed on said front surface of said submount substrate, said first common terminal being electrically connected to said each one or more first submount contacts;

at least a first conducting via extending from said front surface of said submount substrate to a back surface of said submount substrate, said first conducting via being electrically connected to said first common terminal;

a first further terminal disposed on said back surface of said submount substrate and configured to provide connections external to said submount structure, said first further terminal being electrically connected to said first conducting via;

one or more second submount contact pads, each such one or more second submount contact pads exposed at said front surface of said submount substrate;

a second common terminal disposed on said front surface of said submount substrate, said second common

terminal being electrically connected to said each one or more second submount contacts;

at least a second conducting via extending from said front surface of said submount substrate to said back surface of said submount substrate, said second conducting via being electrically connected to said second common terminal; and

a second further terminal disposed on said back surface of said submount substrate and configured to provide connections external to said submount structure, said second further terminal being electrically connected to said second conducting via.

67. A Schottky diode, comprising:

a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of a same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer, said semiconductor body defining a lower contact surface and a first mesa projecting upwardly from said main surface, said first mesa including at least a portion of said upper layer and defining an upper contact surface, said first mesa having a main portion, at least one bridge extending from said main portion, and a plurality of extensions extending from said main portion or from said bridge, said plurality of extensions being interdigitated with regions of said lower contact surface, said main portion and said bridge being elongated at least in a first direction and at least some of said extensions being elongated in a second direction transverse to said first direction, at least some of said extensions have length-to-width ratios of at least about 2:1;

one or more upper metallic contacts disposed atop said first mesa and forming a Schottky contact with the upper contact surface of said first mesa; and

one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact therewith, at least part of said one or more lower metallic contacts extending between at least some of said plurality of extensions.

68. A Schottky diode as claimed in claim 67 wherein said first mesa has a perimeter at least two times the perimeter of a smallest theoretical rectangle enclosing said first mesa.

69. A Schottky diode as claimed in claim 67 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

70. A Schottky diode as claimed in claim 67 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

71. A Schottky diode as claimed in claim 67 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.

72. A method of forming a Schottky diode, said method comprising:

providing a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of a same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer;

patterning and etching one or more regions of said semiconductor body to define a lower contact surface and a plurality of mesas projecting upwardly from said lower contact surface, said lower contact surface including at least a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and defining an upper contact surface, each of said plurality of mesas being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface;

forming a plurality of upper metallic contacts each disposed atop a respective one of said plurality of mesas and forming a respective Schottky contact with the upper contact surface of that mesa; and

forming one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact

therewith, at least part of said one or more lower metallic contacts extending between at least some of said plurality of mesas.

73. A method as claimed in claim 72 wherein a size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized.

74. A method as claimed in claim 72 wherein each of said plurality of mesas includes a portion of said lower layer.

75. A method as claimed in claim 72 wherein each of said plurality of upper metallic contacts includes a contact metal layer that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

76. A method as claimed in claim 72 wherein each of said one or more lower metallic contacts includes a contact metal layer that forms the ohmic contact with said lower contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

77. A method as claimed in claim 72 wherein said one or more continuous lower metallic contact regions includes one or more continuous regions, each such continuous region extending between two or more of said mesas.

78. A method as claimed in claim 72 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

79. A method as claimed in claim 72 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

80. A method as claimed in claim 72 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.

81. A method as claimed in claim 72 wherein said lower semiconductor layer and said upper semiconductor layer are n-type.

82. A method as claimed in claim 72 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a convoluted perimeter.

83. A method as claimed in claim 82 wherein said perimeter of said shape is at least two times a perimeter of a smallest theoretical rectangle enclosing said shape.

84. A method as claimed in claim 72 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion and a plurality of extensions extending from said main portion, said plurality of extensions being interdigitated with regions of said lower contact surface.

85. A method as claimed in claim 84 wherein said main portion is elongated at least in a first direction and at least some of said plurality of extensions are elongated in a second direction transverse to said first direction.

86. A method as claimed in claim 84 wherein at least some of said plurality of extensions have length-to-width ratios of at least about 2:1.

87. A method as claimed in claim 84 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

88. A method as claimed in claim 84 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

89. A method as claimed in claim 72 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion, at least one bridge extending from said main portion and a plurality of extensions extending from said bridge; said plurality of extensions being interdigitated with regions of said lower contact surface.

90. A method as claimed in claim 89 wherein said main portion and said bridge are elongated at least in a first direction and at least some of said extensions are elongated in a second direction transverse to said first direction.

91. A method as claimed in claim 89 wherein at least some of said extensions have length-to-width ratios of at least about 2:1.

92. A method as claimed in claim 89 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

93. A method as claimed in claim 89 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

94. A method of forming a Schottky diode, said method comprising:

providing a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of the same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer;

patterning and etching one or more regions of said semiconductor body to define a lower contact surface and a plurality of mesas projecting upwardly from said lower contact surface, said lower contact surface including a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and a further portion of said lower layer, each of said plurality of mesas defining an upper contact surface and being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface;

a plurality of upper metallic contacts each disposed atop a respective one of said plurality of mesas and forming a

respective Schottky contact with the upper contact surface of that mesa; and

one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact therewith.

95. A method as claimed in claim 94 wherein a size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized.

96. A method as claimed in claim 94 wherein the distance between a top surface of said one or more lower metallic contacts and said lower contact surface is less than the distance between a bottom surface of said upper layer and said lower contact surface.

97. A method as claimed in claim 94 wherein each of said plurality of upper metallic contacts includes a contact metal layer that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

98. A method as claimed in claim 94 wherein each of said one or more lower metallic contacts includes a contact metal layer that forms the ohmic contact with said lower contact surface and a bond pad metal layer that is disposed atop said contact metal layer.

99. A method as claimed in claim 94 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

100. A method as claimed in claim 94 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

101. A method as claimed in claim 94 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.

102. A method as claimed in claim 94 wherein said lower semiconductor layer and said upper semiconductor layer are n-type.

103. A method as claimed in claim 94 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a convoluted perimeter.

104. A method as claimed in claim 103 wherein said perimeter of said shape is at least two times a perimeter of a smallest theoretical rectangle enclosing said shape.

105. A method as claimed in claim 94 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion and a plurality of extensions extending from said main portion, said plurality of extensions being interdigitated with regions of said lower contact surface.

106. A method as claimed in claim 105 wherein said main portion is elongated at least in a first direction and at least some of said plurality of extensions are elongated in a second direction transverse to said first direction.

107. A method as claimed in claim 105 wherein at least some of said plurality of extensions have length-to-width ratios of at least about 2:1.

108. A method as claimed in claim 105 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

109. A method as claimed in claim 105 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

110. A method as claimed in claim 94 wherein at least some of said plurality of mesas intersect with at least another of said plurality of mesas and define a shape having a main portion, at least one bridge extending from said main portion and a plurality of extensions extending from said bridge; said plurality of extensions being interdigitated with regions of said lower contact surface.

111. A method as claimed in claim 110 wherein said main portion and said bridge are elongated at least in a first direction and at least some of said extensions are elongated in a second direction transverse to said first direction.

112. A method as claimed in claim 110 wherein at least some of said extensions have length-to-width ratios of at least about 2:1.

113. A method as claimed in claim 110 wherein at least one of said plurality of upper metallic contacts is disposed atop said main portion.

114. A method as claimed in claim 110 wherein at least some of said plurality of upper metallic contacts are disposed atop at least some of said plurality of extensions and are electrically connected with one another, and said at least part of said one or more lower metallic contacts extends between at least said some of said plurality of extensions.

115. A method of forming a Schottky diode, said method comprising:

providing a semiconductor body including a lower semiconductor layer and an upper semiconductor layer formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of a same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer;

patterning and etching one or more regions of said semiconductor body defining a lower contact surface and a first mesa projecting upwardly from said main surface, said first mesa including at least a portion of said upper layer and defining an upper contact surface, said first mesa having a main portion, at least one bridge extending from said main portion, and a plurality of extensions extending from said main portion or from said bridge, said plurality of extensions being interdigitated with regions of said lower contact surface, said main portion and said bridge being elongated at least in a first direction and at least some of said extensions being elongated in a second direction transverse to

said first direction, at least some of said extensions have length-to-width ratios of at least about 2:1;

forming one or more upper metallic contacts disposed atop said first mesa and forming a Schottky contact with the upper contact surface of said first mesa; and

forming one or more lower metallic contacts disposed on said lower contact surface in substantially ohmic contact therewith, at least part of said one or more lower metallic contacts extending between at least some of said plurality of extensions.

116. A method as claimed in claim 115 wherein said first mesa has a perimeter at least two times the perimeter of a smallest theoretical rectangle enclosing said first mesa.

117. A method as claimed in claim 115 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a nitride-based semiconductor.

118. A method as claimed in claim 115 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes a gallium nitride-based semiconductor.

119. A method as claimed in claim 115 wherein at least one of said upper semiconductor layer and said lower semiconductor layer includes GaN.